WHAT IS CLAIMED IS:

1. A clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, said clock adjustment apparatus comprising:

a phase error calculation circuit calculating the phase error of the clock signal based on the sampled values of the readout signal.

2. The clock adjustment apparatus as claimed in claim 1, wherein the readout signal successively comprises a first, a second and a third sampled value in an order sampled, and said phase error calculation circuit calculates the phase error based on a difference between an absolute value of a difference between the first and second sampled values and an absolute value of a difference between the second and third sampled values.

3. The clock adjustment apparatus as

claimed in claim 1, wherein said phase error calculation circuit continuously calculates the phase error based on all of successive sampled values in an acquisition mode in which pattern data having a highest density is reproduced.

4. The clock adjustment apparatus as claimed in claim 1, further comprising:

an edge detection circuit detecting an edge portion of the readout signal based on the transition state of the sampled values of the readout signal,

wherein said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the edge portion of the readout signal detected by said edge detection circuit.

5. The clock adjustment apparatus as claimed in claim 4, wherein:

said edge detection circuit includes a rising edge detection circuit which detects a rising edge portion of the readout signal; and

said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the rising edge portion of the readout signal detected by said rising edge detection circuit.

6. The clock adjustment apparatus as claimed in claim 4, wherein:

said edge detection circuit includes a falling edge detection circuit which detects a falling edge portion of the readout signal; and

said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the falling edge portion of the readout signal detected by said falling edge detection circuit.

7. The clock adjustment apparatus as claimed in claim 4, wherein said edge detection circuit detects a portion of the readout signal as the edge portion when the portion comprises a series of successive sampled values in ascending order from a value smaller than a predetermined threshold to a value larger than the predetermined threshold, or when the portion comprises a series of successive sampled values in descending order from a value larger than a predetermined threshold to a value smaller than the predetermined threshold.

8. The clock adjustment apparatus as claimed in claim 7, wherein said edge detection circuit detects the portion of the readout signal as the edge portion when the portion comprises a first, a second and a third sampled value in an order sampled with the predetermined threshold being between the first and third sampled values, and a sign of a difference between the first and second

sampled values is equal to that of a difference between the second and third sampled values.

9. The clock adjustment apparatus as claimed in claim 7, wherein:

said edge detection circuit comprises an offset estimation circuit which estimates an offset of the readout signal caused by an envelope variation thereof; and

the predetermined threshold for detecting the edge portion of the readout signal is corrected in accordance with the offset estimated by said offset estimation circuit.

10. The clock adjustment apparatus as claimed in claim 7, further comprising:

a threshold defining circuit defining the predetermined threshold.

11. The clock adjustment apparatus as claimed in claim 4, wherein said phase error calculation circuit operates in an acquisition mode in which the phase error of the clock signal is continuously calculated based on all of successive sampled values of the readout signal and in a tracking mode in which the phase error is calculated based on the sampled values of the edge portion of the readout signal detected by said edge detection

circuit,

said clock adjustment apparatus further comprising an operation mode switching circuit which switches an operation mode of said phase error calculation circuit from the acquisition mode to the tracking mode when an amplitude of the phase error calculated by said phase error calculation circuit remains within a predetermined range for a predetermined period of time in the acquisition mode.

12. The clock adjustment apparatus as claimed in claim 11, wherein said operation mode switching circuit comprises a convergence time setting circuit which sets the predetermined period of time which is used as a reference when switching the operation mode.

13. The clock adjustment apparatus as claimed in claim 11, wherein said operation mode switching circuit comprises a convergence range setting circuit which sets the predetermined range which is used as a reference when switching the operation mode.

14. The clock adjustment apparatus as claimed in claim 11, wherein said phase error calculation circuit comprises a gain adjustment circuit which adjusts a gain according to the phase

error of the clock signal calculated thereby, and employs the adjusted gain to adjust the phase of the clock signal,

said clock adjustment apparatus further comprising a gain switching circuit which sets a first gain with respect to said gain adjustment circuit when said phase error calculation circuit operates in the acquisition mode and a second gain, which is smaller than the first gain, with respect to said gain adjustment circuit when said phase error calculation circuit operates in the tracking mode.

15. The clock adjustment apparatus as claimed in claim 11, wherein:

said data reproduction system comprises an equalizer which performs a waveform equalization on the sampled values of the readout signal; and

said phase error calculation circuit, in the tracking mode, calculates the phase error of the clock signal based on the transition state of the sampled values on which the waveform equalization has been performed by said equalizer.

16. The clock adjustment apparatus as claimed in claim 15, further comprising:

a circuit which prevents the phase of the clock signal from being adjusted based on the phase error calculated by said phase error calculation circuit during a predetermined period of time before and after said phase error calculation circuit

switches from the acquisition mode to the tracking mode.

17. The clock adjustment apparatus as claimed in claim 1, further comprising:

a normalization circuit which normalizes the phase error of the clock signal calculated by said phase error calculation circuit so that a transfer function of a feedback loop for adjusting the phase of the clock signal remains constant.

18. A clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, said clock adjustment apparatus comprising:

a phase error calculation circuit calculating the phase error of the clock signal based on a transition state of the sampled values of the readout signal before undergoing the Viterbi algorithm.

19. An apparatus comprising:

a data reproduction system which samples a readout signal from a recording medium in synchronism with a clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic,

said data reproduction system comprising a clock adjustment circuit comprising a phase error calculation circuit calculating a phase error of the clock signal based on the sampled values of the readout signal, and adjusting a phase of the clock signal based on the phase error.

20. The apparatus as claimed in claim 19, wherein the recording medium is formed by an optical disk.